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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,919	08/27/2003	Shenggao Li	P16582	5068
28062	7590	12/29/2004	EXAMINER	
BUCKLEY, MASCHOFF, TALWALKAR LLC			SHINGLETON, MICHAEL B	
5 ELM STREET			ART UNIT	
NEW CANAAN, CT 06840			PAPER NUMBER	
			2817	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/648,919

Applicant(s)

LI

Examiner

Michael B. Shingleton

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) ____ is/are allowed.
- 6) ☐ Claim(s) 1,2,11-13 and 17-22 is/are rejected.
- 7) ☒ Claim(s) 3-10 and 14-16 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 11 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yabe 2001/0043123 (Yabe).

Figure 6-8 and the relevant text of Yabe discloses a ring oscillator for use in a pll circuit having a plurality of delay cells 10a coupled in series as a ring (Ring oscillator) and a replica cell 11 that includes a differential pair of transistors. Note the diode connected NMOS transistor in 2a and the diode connected NMOS transistor in 1a. The replica cell outputs a bias signal at the output of element 12. Note that this bias signal biases transistors that include Q10 and Q6. The diode connection is what applicant describes as the second terminal connected to the first. Q9 and Q8 met the first and second active resistors for as described by applicant FETs forms active resistors.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 17-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabe 2001/0043123 (Yabe) in view of Iravani 5,936,476 (Iravani).

Figure 6-8 and the relevant text of Yabe discloses a ring oscillator for use in a pll circuit having a plurality of delay cells 10a coupled in series as a ring (Ring oscillator) and a replica cell 11 that includes a differential pair of transistors. Note the diode connected NMOS transistor in 2a and the diode connected NMOS transistor in 1a. The replica cell outputs a bias signal at the output of element 12. Note that this bias signal biases transistors that include Q10 and Q6. The diode connection is what applicant describes as the second terminal connected to the first. Q9 and Q8 met the first and second active resistors for as described by applicant FETs forms active resistors. The operational amplifier of Yabe fails to have the inverting input coupled to the replica cell whereas the non-inverting terminal is coupled to Vref. Note that the VCO of Yabe provides an input to the pll (phase locked loop) in the conventional manner. Yabe also fails to disclose the use of the circuit in an optical transmitter. Clearly Yabe is a component of a larger system.

One well known alternative and art recognized equivalent biasing arrangement to control the biasing of the delay cells and thus the frequency is by an operational amplifier wherein the inverting terminal is connected to the replica circuit and the output is connected to active resistors that control the current through the delay cells as taught by Iravani (See Figure 2).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replace the operational amplifier circuit of Yabe with one that has an operational amplifier wherein the inverting terminal is connected to the drain terminal of the replica circuit and the output is connected to active resistors that control the current through the delay cells given the art recognized equivalence as taught by Iravani.

Yabe is a component of a larger system. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the clock of that made obvious above in a conventional optical transmitter arrangement that includes first and second pll's because, as the references are silent on the exact use of the component one of ordinary skill in the art would have been

motivated to use the component in any art-recognized system that employs pll's or clocks such as the conventional optical transmitter arrangement that includes first and second pll's. Note that applicant describes the invention as being in the replica cell and not the optical transmitter arrangement.

Accordingly, the basic optical transmitter arrangement claimed is seen as conventional.

Claims 12, 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabe 2001/0043123 (Yabe).

Figure 6-8 and the relevant text of Yabe discloses a ring oscillator for use in a pll circuit having a plurality of delay cells 10a coupled in series as a ring (Ring oscillator) and a replica cell 11 that includes a differential pair of transistors. Note the diode connected NMOS transistor in 2a and the diode connected NMOS transistor in 1a. The replica cell outputs a bias signal at the output of element 12. Note that this bias signal biases transistors that include Q10 and Q6. The diode connection is what applicant describes as the second terminal connected to the first. Q9 and Q8 met the first and second active resistors for as described by applicant FETs forms active resistors. The operational amplifier of Yabe fails to have the inverting input coupled to the replica cell whereas the non-inverting terminal is coupled to Vref. Note that the VCO of Yabe provides an input to the pll (phase locked loop) in the conventional manner. Yabe also fails to disclose the use of the circuit in an optical transmitter. Clearly Yabe is a clearly a component of a larger system.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the clock of that made obvious above in a conventional optical transmitter arrangement that includes first and second pll's because, as the references are silent on the exact use of the component one of ordinary skill in the art would have been motivated to use the component in any art-recognized system that employs pll's or clocks such as the conventional optical transmitter arrangement that includes first and second pll's. Note that applicant describes the invention

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as being in the replica cell and not the optical transmitter arrangement. Accordingly, the basic optical transmitter arrangement claimed is seen as conventional.

Claims 3-10 and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

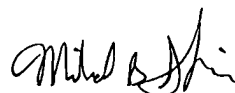
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS

December 24, 2004


MICHAEL B. SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817